Claims:

1. A method for manufacturing electronic thin-film components, said method comprising at least the following steps:

— a substantially dielectric substrate is selected,
— a lowermost, galvanically uniform conductive layer of an electrically conductive material is formed on said substrate,
— conductive areas are galvanically separated from each other from said lowermost conductive layer to form an electrode pattern by exerting on the lowermost conductive layer a machining operation based on die-cut embossing, i.e. embossing, wherein the relief of the machining member used in the machining operation causes a permanent deformation on the substrate and at the same time embosses areas from the conductive layer into conductive areas galvanically separated from each other,
— further, one or several upper passive or active layers required in the thin-film component are formed on top of said electrode pattern,

characterized in that

— conductive areas are formed by said embossing operation exerted on the lowermost conductive layer, said conductive areas being on at least two different levels, which levels have different positions in a direction perpendicular to the plane of the substrate i.e. in the vertical direction.

2. The method according to claim 1, **characterized** in that by means of said embossing operation exerted on the lowermost conductive layer, one or more upper passive or active layers of the thin-film component are formed simultaneously.

3. The method according to claim 1 or 2, **characterized** in that the lowermost conductive layer formed on the substrate, which is to be patterned by means of embossing, is produced by vacuum coating.

4. The method according to claim 3, **characterized** in that said vacuum coating and embossing are performed in the same vacuum process.

5. The method according to any of the preceding claims, **characterized** in that one of the following materials or a laminated combination thereof is selected:. plastic, glass, paper or paperboard.

6. The method according to claim 5, **characterized** in that the substrate material is heated for the embossing.

7. The method according to claim 6, **characterized** in that when the substrate material contains plastic, the embossing of said lowermost conductive layer is performed at a temperature, which is slightly above the glass transition temperature of said plastic material.

8. The method according to any of the preceding claims, **characterized** in that one of the following materials or a combination thereof is selected as the material of the lowermost conductive layer: transparent or non-transparent semiconducting oxide, metal, conductive ink or conductive polymer.

9. The method according to any of the preceding claims, **characterized** in that the vertical depth of the machining member used in embossing and/or the horizontal line widths used therein are selected from the range 1 to 50 μm.

10. The method according to any of the preceding claims, **characterized** in that the relief of the machining member used in the embossing is selected so that it has substantially upright walls in the vertical direction.

11. The method according to any of the preceding claims, **characterized** in that a nickel pressing block or plate is used as the machining member in the embossing, the relief of the master or the like of said

block or plate being formed by means of direct resist lithography or a combination of resist lithography and dry etching technique.

12. The method according to any of the preceding claims, **characterized** in that at least some of the process stages described in the claims above are performed in the same roll-to-roll process.

13. The method according to any of the preceding claims, **characterized** in that the electrode pattern formed by means of embossing or the upper passive or active layers formed simultaneously by means of embossing are post-treated by means of a plasma processing.

14. An apparatus for manufacturing electronic thin-film components on a substantially dielectric substrate, said apparatus comprising at least

— first growing means for growing a lowermost, galvanically uniform conductive layer of an electrically conductive material on said substrate,

— patterning means for galvanically separating the conductive areas from each other from said lowermost conductive layer to form an electrode pattern, said patterning means being embossing means based on die-cut embossing, i.e. embossing, said means comprising at least one machining member whose relief causes a permanent deformation on the substrate and at the same time embosses areas from the conductive layer into conductive areas galvanically separated from each other,

— second growing means for forming one or several upper passive or active layers required in a thin-film component on top of said electrode pattern,

characterized in that

— said patterning means are arranged to form conductive areas by said embossing operation exerted on the lowermost conductive layer, said conductive areas being on at least two different levels, which levels have different positions in a direction perpendicular to the plane of the substrate i.e. in the vertical direction.

15. The apparatus according to claim 14, **characterized** in that said patterning means are arranged to form one or several upper passive or active layers of the thin-film component simultaneously by means of said embossing operation exerted on the lowermost conductive layer.

16. The apparatus according to claim 14 or 15, **characterized** in that said first growing means for forming the lowermost conductive layer to be patterned by means of embossing on the substrate are vacuum coating means.

17. The apparatus according to claim 16, **characterized** in that said vacuum coating means and embossing means are arranged in the same vacuum process.

18. The apparatus according to any of the preceding claims 14 to 17, **characterized** in that the vertical depth of the relief of the machining member used in embossing and/or the horizontal line widths used therein are in the range 1 to 50 μm.

19. The apparatus according to any of the preceding claims 14 to 18, **characterized** in that the relief of the machining member used in the embossing is arranged so that it has substantially upright walls in the vertical direction.

20. The method according to any of the preceding claims 14 to 19, **characterized** in that the machining member used in the embossing is a nickel pressing block or plate, the relief of the master or the like of said machining member being formed by means of direct resist lithography or a combination of resist lithography and dry etching technique.

21. The apparatus according to any of the preceding claims 14 to 20, **characterized** in that at least said first growing means and said patterning means are arranged to be in the same roll-to-roll process.

22. An electronic thin-film component comprising at least

- a substantially dielectric substrate,
- a lowermost conductive layer of an electrically conductive material formed on said substrate, which
- said conductive layer is patterned into conductive areas galvanically separated from each other and forming an electrode pattern by exerting on the lowermost conductive layer a machining operation based on die-cut embossing, i.e. embossing, wherein the relief of the machining member used in the machining operation causes a permanent deformation on the substrate and at the same time embosses areas from the conductive layer into conductive areas separated from each other galvanically,
- one or several upper passive or active layers formed on top of said electrode pattern,

characterized in that

- the component comprises conductive areas formed by said embossing operation, said conductive areas being formed from the lowermost conductive layer, and said conductive areas being on at least two different levels, which levels have different positions in a direction perpendicular to the plane of the substrate i.e. in the vertical direction.

23. The component according to claim 22, **characterized** in that the component comprises one or several upper passive or active layers, which are formed by the same embossing operation exerted on the lowermost conductive layer.

24. The component according to claim 22 or 23, **characterized** in that the material of said substrate is one of the following materials or a laminated combination thereof: plastic, glass, paper or paperboard.

25. The component according to any of the preceding claims 22 to 24, **characterized** in that the material of the lowermost conductive layer is one of the following or a combination thereof: transparent or non-transparent semiconducting oxide, metal, conductive ink or conducting polymer.

26. The component according to any of the preceding claims 22 to 25, **characterized** in that the horizontal line widths of the electrode pattern formed in the lowermost conductive layer by means of embossing or the distance between the electrode patterns in the vertical depth direction is in the range 1 to 50 μm.

27. The component according to any of the preceding claims 22 to 26, **characterized** in that the component comprises at least one upper active layer formed on top of said electrode pattern, the material of said layer being an organic or inorganic semiconducting material.

28. The component according to claim 27, **characterized** in that said at least one upper active layer is arranged to form one of the following structures: a channel structure of a transistor, a photoactive layer of a solar cell or a photocell, an electroluminescent layer of a light-emitting component.

29. The component according to any of the preceding claims 22 to 28, **characterized** in that the component is one of the following: a light emitting diode, a field effect transistor, an active or passive pixel display, a photocell or a solar cell.

30. The component according to any of the preceding claims 22 to 29, **characterized** in that the component comprises one or more upper passive or active layers, whose vertical dimension with respect to the plane of the substrate is determined by the embossing operation exerted on the lowermost conductive layer.

31. The component according to claim 30, **characterized** in that the component is an organic field effect transistor OFET, the length (L) of whose channel structure is determined by embossing in the vertical direction with respect to the plane of the substrate.

32. The component according to any of the preceding claims 22 to 31, **characterized** in that the component is a pixel display based on

organic light emitting diodes OLED, in which individual pixels of the display are formed in the intersections of crossing stripe-like electrodes representing different polarities, and in which component parallel adjacent electrodes representing the same polarity are formed on different levels with respect to the substrate in the vertical direction.

33. The component according to claim 32, **characterized** in that vertical distance between said parallel adjacent electrodes representing the same polarity is in the range 1 to 5 μm.